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ABSTRACT OF THE DISCLOSURE

To synchronize a regularly occurring pulse train to the average of a bunched pulse train, an oscillator generates a plurality of differently phase shifted signals at a given frequency. One of the phase shifted signals is selected as an output signal. The output signal is compared with the bunched pulse train. The selected phase shifted signal is changed responsive to the comparison so the output signal occurs at the average frequency of the bunched pulse train. The oscillator is formed as a plurality of differential amplifier stages having equal controllable delays. The stages are connected together to form a ring oscillator. The output signal is compared with the bunched pulse train through a A signal representative of the state of the FIFO is used as an error signal to control the selection of the phase shifted signal to be used as the output signal. locked loop that synchronizes the phase shifted signal generating oscillator to a frequency reference is nested in the control loop that selects one of the phase shifted signals as the output signal.

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